**-- 4 bit Synchronous mode control up/down counter – behavioral**

**1. Code**

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity Mode\_control\_counter is

Port ( clk,cr,pr,mode : in STD\_LOGIC;

q : out STD\_LOGIC\_VECTOR (3 downto 0));

end Mode\_control\_counter;

architecture Behavioral of Mode\_control\_counter is

signal tmp: std\_logic\_vector(3 downto 0);

begin

process (clk, cr,pr)

begin

if (cr='0') then

tmp <= "0000";

elsif (pr ='0') then

tmp <= "1111";

elsif (clk'event and clk='1') then

if (mode='1') then

tmp <= tmp - 1;

else

tmp <= tmp + 1;

end if;

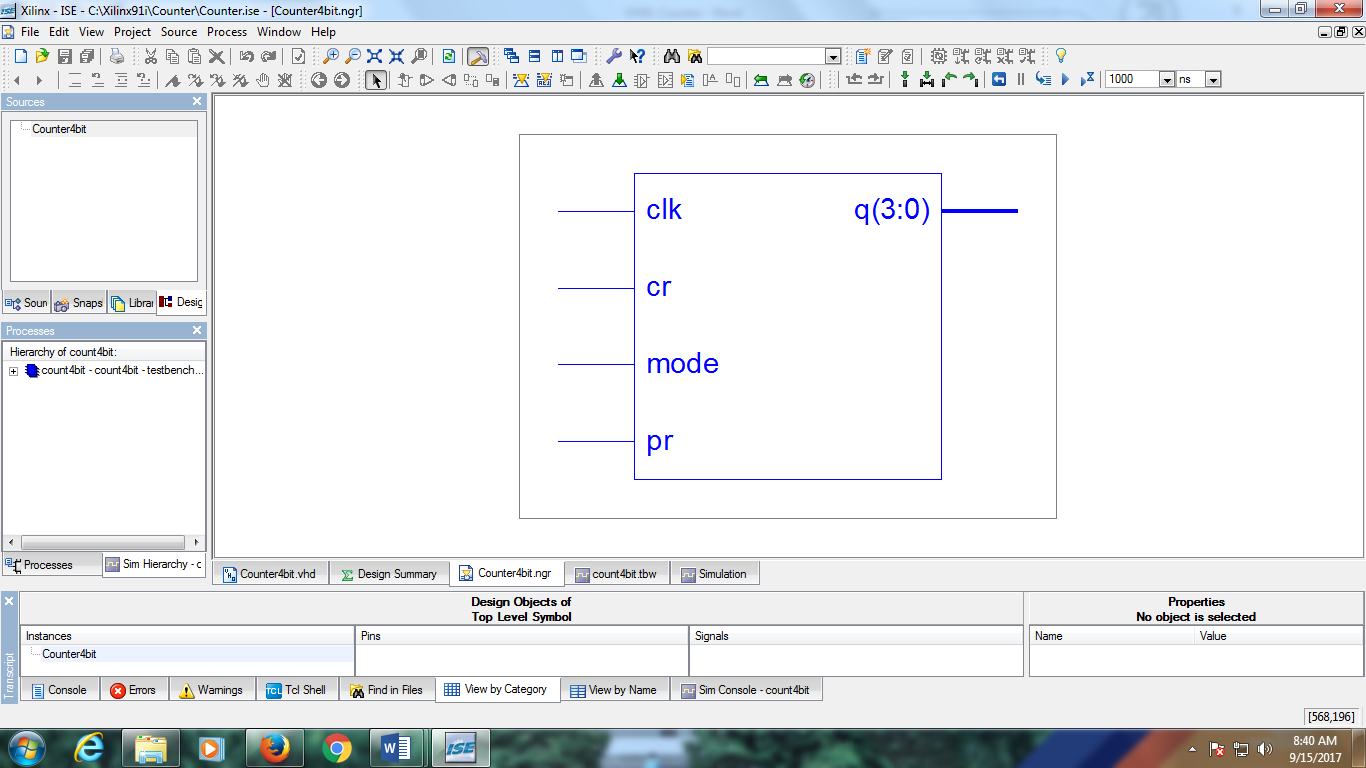
end if;

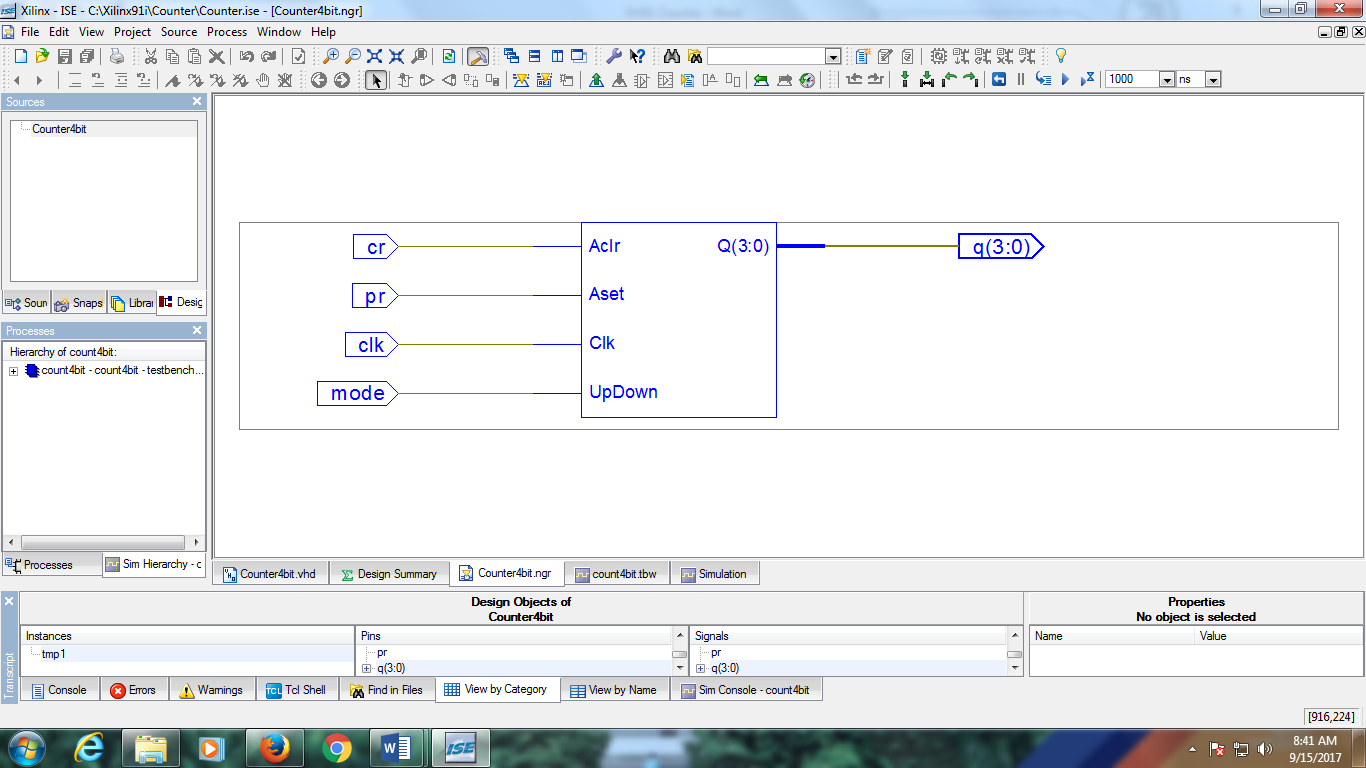
end process;

q <= tmp;

end Behavioral;

**2. RTL Schematic**





**3. Simulation Output**

